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DSI3 Bus Standard

Revision 1.00

February 16, 2011

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1 INTRODUCTION

94

1.1 DSI3 General Overview

95

96 This document defines the 3rd generation Distributed System Interface (DSI3). It documents the bus topologies,
97 operational modes and functional classes of DSI3 bus systems and the associated electrical and physical characteristics.
98 It also defines the message protocol, message transaction models, message formats, bit transmission order and message
99 error checking.

100 DSI3 is a third generation satellite interface bus primarily intended for safety critical communication between a central
101 master interface and multiple satellite nodes, also called slaves. Slave nodes can be implemented as simple state
102 machines or as microprocessor or DSP based controllers. The slaves can provide raw data signal sources or pre-
103 processed signal sources. Each slave can contain a single data source or multiple data sources. Slave nodes can also
104 provide output and control functions.

105 Included within the DSI3 protocol is a Discovery Mode whereby slave devices automatically determine their position
106 on a serial daisy-chain bus and each slave is assigned a unique physical address. The Discovery Mode allows for the
107 identification of slaves with identical features and part number according to their position on the serial daisy-chain bus.
108 For slaves with unique characteristics, the Discovery Mode can be used to ensure that the device with the correct
109 capability is in the proper location of the serial daisy-chain bus.

110 DSI3 includes a fail silent philosophy and an optional Background Diagnostic Mode that operates during normal
111 periodic sampling mode. The Background Diagnostic Mode provides advanced services for diagnostics and functional
112 safety. The fail silent philosophy is enhanced by Background Diagnostic Mode.

113 The primary target application area for the DSI3 network is automotive airbag systems however it is anticipated that the
114 new features of the protocol will allow the use of DSI3 in other application areas.

1.2 DSI3 Protocol Main Features

115

116 The fundamental strengths of previous DSI versions remain and new elements have been adopted where necessary to
117 meet the expanded goals of an improved bus standard. Lessons learned from previous DSI versions, competing
118 strategies and the expectations of users have been considered in the development of DSI3.

119 DSI3 provides an efficient bi-directional communication scheme by means of forward and reverse channels. The
120 forward communication channel defines master to slave communication and the reverse communication channel
121 defines slave to master communication. The forward and reverse communication channels operate at half-duplex in
122 contrast to previous versions of the protocol. Several modes of operation are provided to optimize performance of both
123 the forward and reverse communication channels to match the needs of the application. All modes are synchronous
124 since all transactions are initiated by the master.

125 The DSI3 protocol has been designed to improve upon the capabilities of all existing sensor bus protocols. In
126 particular there are bandwidth improvements, EMC improvements and data integrity improvements. There are also
127 fundamental changes that allow for reduced cost implementations.

1.2.1 DSI3 Bandwidth Improvements

128

129 Bandwidth improvements are the result of an efficient Time-Division-Multiple-Access (TDMA) method utilizing
130 multi-level source coding of the response signal, a global clock management scheme, an optimized reverse channel
131 strategy and an increased bit-rate.

132 **1.2.2 EMC Improvements**

133 DSI3 includes fundamental changes designed to improve electromagnetic compatibility. EMC improvements are
134 achieved by reducing the master induced voltage fluctuations on the bus. For DSI3 the reduction in the number of
135 master induced voltage fluctuations occurs as a result of a preconfigured periodic response stream. The fundamental
136 frequency of the master induced voltage fluctuations has been reduced by nearly two orders of magnitude (from
137 200kHz to approximately 4kHz) compared with previous versions of DSI, resulting in further significant AM band
138 emissions reductions.

139 **1.2.3 Data Integrity Improvements**

140 The DSI3 Protocol has features designed to address the requirements of safety critical communications. In particular
141 there are mechanisms built in to improve the safety case of the protocol. Examples of the mechanisms include: source
142 identification, Background Diagnostic Mode, keep alive counters, and increased error detection capability.

143 **1.2.4 Cost Controls**

144 The DSI3 Protocol adopts a philosophy that allows system and device implementers to scale the protocol to meet the
145 specific requirements of an application. The protocol can be scaled in several dimensions whereby a base functionality
146 is extended with additional features to meet more demanding or varied applications.

147 **1.3 Use of the standard and Legal Information**

148 This specification was developed within the DSI Consortium (“DSI”). Use of this specification is voluntary and is
149 subject to the DSI Consortium Bylaws and Membership Agreement.

150 This specification is supplied “AS IS.” DSI Disclaims liability for any personal injury, property, or other damage, of
151 any nature whatsoever, whether special, indirect, consequential, or compensatory, directly or indirectly resulting from
152 the publication, use of, or reliance upon this, or any other DSI document. DSI makes no warranties or representations
153 as to the accuracy or content of the material contained herein, and expressly disclaims any express or implied warranty,
154 including any implied warranty of merchantability or fitness for a specific purpose, or that the use of the material
155 contained herein is free from patent infringement.

2 DSI3 Bus Topologies, Functional Classes and Operational Modes

2.1 Overview

The DSI3 protocol manages the formation of networks consisting of a *master* node and one or more *slave* nodes. A system can consist of one or more master nodes. Communication between the master and slaves follows a command and response transaction model with a separate *command phase* and *response phase*. The interconnection of a master node and one or more slave nodes is defined by a bus topology. The DSI3 protocol defines point-to-point, serial daisy-chain and parallel bus topologies.

The DSI3 protocol defines two functional classes of bus operation: the Signal Function Class and the Power Function Class. The Signal Function Class is optimized for periodic data collection from data sources. Signal Function Class slaves can also provide outputs to control logic level functions within the limits and restrictions placed on quiescent current of the Signal Function Class. The Power Function Class is optimized to support power outputs but also supports data sources. The Power Function Class utilizes an additional *power-phase* to supply bus power to the output loads. For the Power Function Class, current draw restrictions place limits on when current is allowed to flow into the loads. Generally the Signal Function Class and the Power Function Class must maintain a constant quiescent current draw during at least the response phase but typically for both the command and response phases. In the context of this specification Power Function Class implies that a slave controls a load and isolates the response communication current draw from the master supplied load current delivered into a power output.

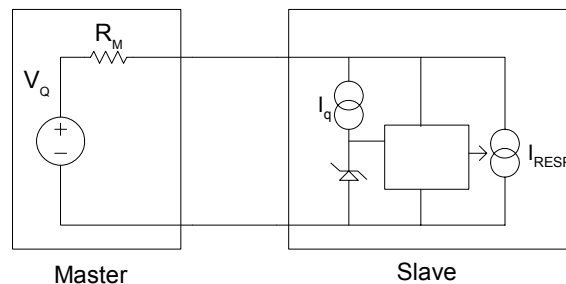
The DSI3 protocol provides several modes of operation. These are broadly divided into a Command and Response Mode and a Periodic Data Collection Mode. For Signal Function Class devices, the Command and Response Mode is utilized to start and configure the bus and thereby form the network. For an application that requires immediate functionality at power-on, a pre-programmed configuration can be loaded into non volatile slave memory. In this case the necessary bus configuration and network formation is available immediately after bus start-up. The Periodic Data Collection Mode is entered after bus initialization, configuration and network formation. The Periodic Data Collection Mode also defines an optional Background Diagnostic Mode for low speed diagnostics that occurs without interrupting the periodic data collection.

For Power Function Class devices, the Command and Response Mode is used to control and monitor outputs and data sources. The Periodic Data Collection Mode is not intended for the Power Function Class.

184 2.2 Bus Topologies

185 2.2.1 Point-to-Point Bus Topology

186 The point to point topology consists of a single master node and a single slave node. For the Signal Function Class the
 187 slave node can contain a single data source or multiple data sources. For the Power Function Class the slave node
 188 provides output signals and optionally data sources. The wiring between the master and the slave are typically twisted
 189 pairs and supply both communication signals and the quiescent current for basic slave internal operation. For Power
 190 Function Class devices, power is delivered through an additional power phase.



191

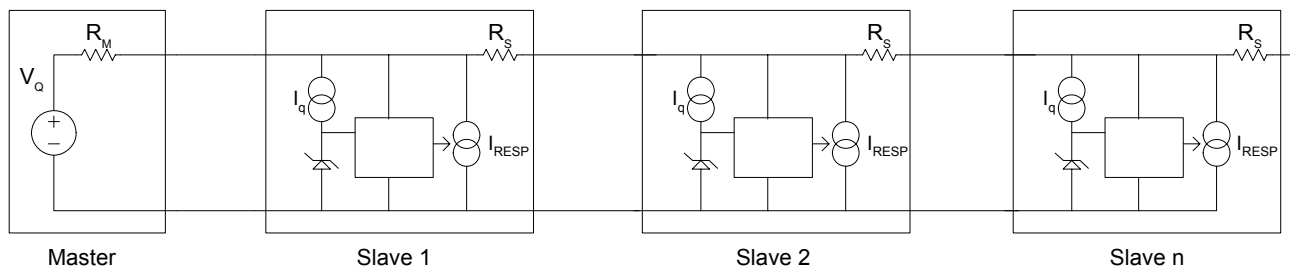
192

Figure 2-1: Point to Point Topology

193 2.2.2 Daisy-Chain Bus Topology

194 The fundamental application for the daisy-chain topology is to determine relative position within a series
 195 interconnection of potentially identical slaves. This can be accomplished with either a series sense resistor or a series
 196 bus switch.

197 If series sense resistors are used, the Discovery Mode determines a slave's relative position in the serial daisy-chain and
 198 manages address assignment during network formation. Typically slaves on a daisy-chain bus are assigned a physical
 199 address at the time of network formation after bus power-up. Alternately the slaves can be pre-programmed with a
 200 physical address and verified via Discovery Mode.



201

202

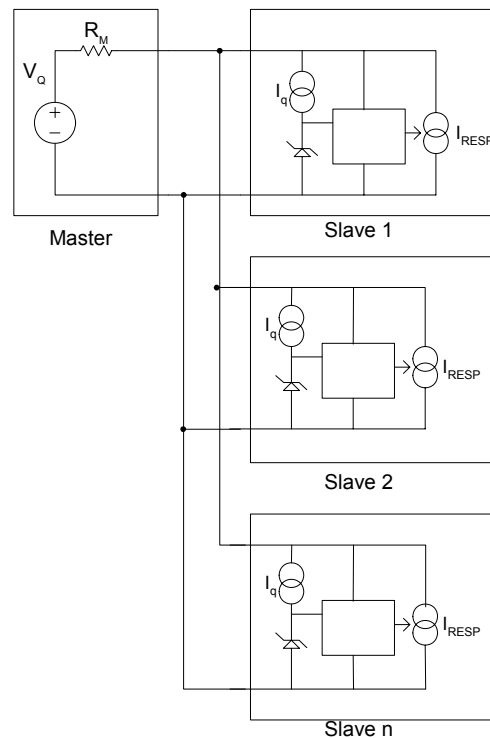
Figure 2-2: Daisy Chain Topology with Sense Resistors

203 The serial daisy-chain can implement a bus switch in lieu of or in addition to the sense resistor. The use of a bus switch
 204 allows isolation of faulted portions of the bus in applications that require fault isolation. A bus switch allows
 205 connection of separate bus segments connected via the bus switch. The Discovery Mode acts on (discovers) individual
 206 segments and each segment is discovered separately. When a bus switch is encountered at the end of a bus segment,
 207 the master commands the slave to close the bus switch to connect the additional slaves to the bus. The new slaves are
 208 discovered as each additional bus segment is connected. The master has a priori knowledge of the bus switches and
 209 therefore the segmented bus architecture. The Discovery Mode is described later in this specification.

210

211 2.2.3 Parallel Bus Topology

212 The parallel bus topology requires pre-programmed physical addresses. The main application for the parallel bus is to
 213 limit the voltage drops along the bus and allow for more slave nodes on the bus.



214

215

Figure 2-3: Parallel Bus Topology

216 The parallel connections can be implemented at the master side, the slave side or in the wire harness. When
 217 implemented in the master side the master must provide the connection pins required for the required number of slaves
 218 and make the pass thru trace connections. When implemented on the slave side the slave must provide the necessary
 219 interconnection pins and the pass thru trace connections. When implemented in the harness the parallel connections are
 220 typically splices.

221 The decision of where to make the parallel connections is an implementation choice and can impact the total system
 222 level costs. The DSI3 protocol allows complete freedom of choice in the connection strategy of the parallel
 223 connections.

224 The parallel connected slaves may include a bus switch. In this case the bus switches can connect new bus segments.
 225 These new bus segments are discovered as described above for additional segments within a serial daisy-chain.

226

2.3 Functional Classes of Operation

2.3.1 Signal Function Class

The Signal Function Class is optimized for applications that prioritize high speed periodic data collection. Signal Function Class slaves can implement single or multiple data sources at each slave node. The Signal Function Class can utilize either the Command and Response Mode or the Periodic Data Collection Mode or a combination of both modes. For example a pre-configured parallel connected network could transition immediately into the Periodic Data Collection Mode. Whereas a serially connected daisy-chain bus would use the Command and Response Mode along with the Discovery Mode to form and configure the network and then transition into the Periodic Data Collection Mode.

As mentioned in section 2.1 there are restrictions on Signal Function Class quiescent current levels. The fundamental restriction is that the quiescent current must remain relatively constant during the response phase within the limits specified in Section 4.3. For Signal Function Class slaves the power supply is generally designed to draw constant quiescent current for both the command and response phase as well as manage inrush current, energy extraction and energy storage for micro-break backup purposes.

2.3.2 Power Function Class

The Power Function Class is optimized for applications with control functions that require power and current levels that cannot be supported by the Signal Function Class. The Power Function Class utilizes the command phase and the response phase with the addition of a power phase. The Power Function Class controls output loads by coordinating the state of output signals during the command phase, the response phase and the power phase. Power Function Class slaves can implement single or multiple output sources. Power Function Class slaves require an energy extraction mechanism that provides isolation between the power phase and the command and response phases.

For Power Function Class slaves the same fundamental restriction for Signal Function Class slaves applies: the quiescent current must remain relatively constant (or essentially zero) during the response phase, within the limits specified Section 4.3. During the power phase the Power Function Class must provide isolation between the voltage level associated with the power phase and the voltage levels during the command and response phases.

252

2.4 Modes of Operation

2.4.1 Signal Function Class: Command and Response Mode

The Command and Response Mode (CRM) is used for network formation and bus configuration for Signal Function Classes. The Command and Response Mode provides services that allow for the reading of and writing to slave memory and changing the internal state of the slave. The Command and Response Mode format is defined in Section 5 of this specification.

The following figure represents the Command and Response Mode timing philosophy for the Signal Function Class. The command signals are Manchester encoded voltage levels defined as V_{HIGH} and V_{LOW} . The response signals are multi-level source encoded currents modulated on top of the total slave quiescent current that is present during the response phase. The command and response timings, voltages, currents and encodings are described in Section 4 of this specification.

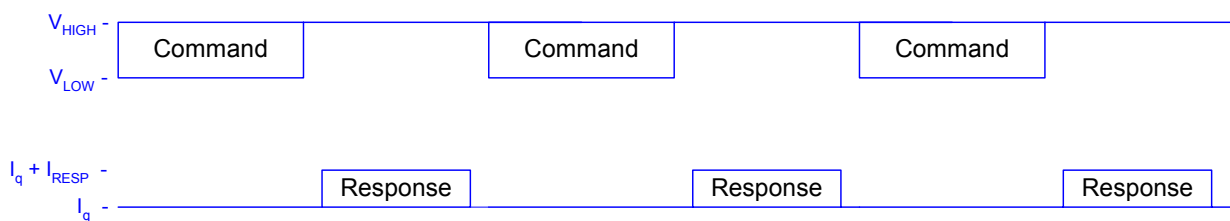


Figure 2-4: Signal Function Class - Command and Response Mode

2.4.2 Signal Function Class: Periodic Data Collection Mode

The Periodic Data Collection Mode (PDCM) is optimized for applications that require high speed synchronous data collection. In the context of this specification synchronous data collection means that the data samples are synchronized by the master through synchronization events. The actual data samples are therefore synchronous with the master synchronization event however the data samples may or may not be simultaneous. The distinction between simultaneous sampling and synchronous sampling is addressed by the implementation and is not controlled by this specification. This allows the system implementer to either choose simultaneous sampling or prioritize the relative latency of the data sources.

The following figure represents the command and response timing philosophy for the Periodic Data Collection Mode. The command transmitted by the master can be either a single bit Broadcast Read Command or a Background Diagnostic Mode command. The commands are Manchester encoded using the same voltage levels defined for the commands used during the Command and Response Mode. The response signals are multi-level source encoded currents assembled into packets modulated on top of the total slave quiescent current. Furthermore the response packets from multiple data sources are time multiplexed utilizing a TDMA approach and separated by inter-packet separations. The command and response timings, inter packet separation timings, voltages, currents and encodings are further described in Sections 4 and 5 of this specification.

For the Periodic Data Collection Mode the protocol requires that the master node be synchronized with the ECU's clock and must meet the timing requirements as defined in Section 4 of this specification.

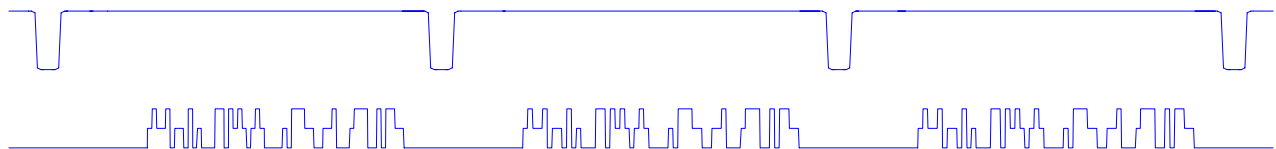
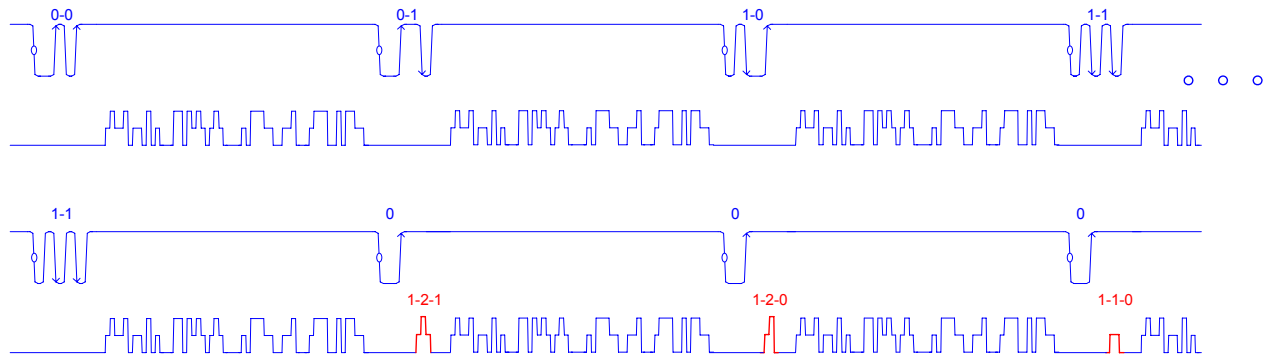


Figure 2-5: Signal Function Class - Periodic Data Collection Mode

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2.4.3 Signal Function Class: Background Diagnostic Mode

An optional low speed diagnostic communication channel called Background Diagnostic Mode (BDM) is defined within the DSI3 specification. The Background Diagnostic Mode does not interfere with the Periodic Data Collection Mode; however the system implementer must reserve some bandwidth for the Background Diagnostic Mode. The reserved bandwidth always starts at the beginning of the sample period. The percentage of the sample period reserved can be adjusted to meet the needs of the application. The forward and reverse data packets are split into sequential parts that are transmitted during consecutive periods – first the command bits and then the response bits. The reserved bandwidth is shared between the low speed forward channel and the corresponding low speed reverse channel. The Background Diagnostic Mode provides services for data integrity functionality and uses a different response format and error detection format. This prevents the classic masquerade phenomena that could lead to misinterpretation of data.



296

297 **Figure 2-6: Signal Function Class - Background Diagnostics Mode Command and Response Bits**

298 Figure 2-6 shows a portion of a command sequence along with the normal periodic responses and a Background
 299 Diagnostic Mode response. In the example shown in Figure 2-6 there are two command bits sent every period (0-0, 0-
 300 1, 1-0 and 1-1). The command (complete command not shown) is followed by the response. The first three response
 301 symbols are shown (1-2-1, 1-2-0, and 1-1-0). As in Periodic Data Collection Mode, each of the response symbols is a
 302 coded representation of a corresponding 4-bit data nibble. The format for the command and response messages is
 303 covered in Section 5.2.3.

304 The bit-rate of the Background Diagnostic Mode is determined by the number of forward and reverse channel bits that
 305 can be transmitted in the time reserved. An example Background Diagnostic Mode configuration may use the
 306 following:

- 307 • 10% of a 250uS sample period reserved for Background Diagnostic Mode
- 308 • A reverse chip time of 3 us. The forward bit time is fixed at 8 us.

309 With this configuration, 2 command bits or 4 response bits can be sent every 250uS. This results in a Background
 310 Diagnostic Mode with an 8kbps forward bit-rate and a 16kbps reverse bit-rate. One 32-bit diagnostic command and one
 311 32-bit diagnostic response can occur in every 6mS period of time.

312 Complex transactions are also possible whereby multiple slaves respond in successive sample intervals in the case of a
 313 broadcast diagnostic request. In the case of a broadcast command, once the command is transmitted, the slaves transmit
 314 their complete response in sequential order based on their source identification, starting from Source ID = 1.

315

316 2.4.4 Power Function Class: Command and Response Mode

317 The Command and Response Mode is used for network formation, bus configuration and actuator controls for the
 318 Power Function Class. The following figure represents the Command and Response Mode timing philosophy for the
 319 Power Function Class. The Power Function Class uses the same command phase and response phase formats as the
 320 Signal Function Class. The command signals are Manchester encoded voltage levels defined as $V_{\text{HIGH-PWR}}$ and $V_{\text{LOW-PWR}}$.
 321 V_{PWR} . The power phase is implemented as an additional bus level defined as V_{IDLE} . The response signals are multi-level
 322 source encoded currents. The response current signals are required to be isolated from the slave load current. The
 323 required isolation of response current from load current is a consequence of the energy extraction used for the Power
 324 Function Class. The command and response timings, voltages, currents and encodings are described in Section 4 of
 325 this specification.

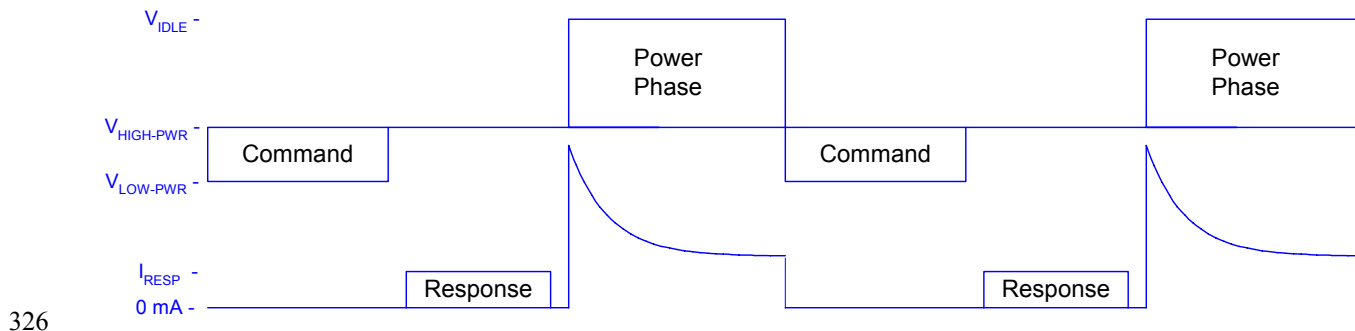


Figure 2-7: Power Function Class - Command and Response Mode

328

3 DSI3 Scalability

329 The DSI3 protocol is scalable in several dimensions. In addition to choosing the functional classes and modes of
330 operation, the device and system implementers can scale additional elements of the DSI3 protocol to meet the system
331 requirements. Typically the protocol is scaled according to the target function class and the overall required
332 performance of the system. As the performance goals are expanded, elements of the protocol can added or scaled to
333 meet new requirements. The scalability allows optimization of cost versus performance. Within the context of the
334 protocol scalability the resultant system performance is based on the lowest common capability in a *controlling*
335 *dimension*. DSI3 systems may accommodate slaves with lower levels of performance in some of the scalable
336 dimensions. Scalable dimensions include the following:

- 337 1. The minimum and maximum operating voltages can be defined by the system implementers within the limits
338 specified in Section 4.2. The minimum and maximum voltage capability of the resulting system is derived
339 from the least capable device on the bus.
- 340 2. The number of slaves in a system is based on the supply current capability and current limit of the master
341 device and can be defined by the system implementer within the limits specified in Section 4.2.1 and Section
342 4.3.1. The system must be designed such that it does not exceed the ratings of the least capable device on the
343 bus. Slaves designed with a lower fault current capability could be damaged if used in a system that could
344 supply higher fault current.
- 345 3. The sample rate of the system can be defined by the system implementers. The sample rate is a function of the
346 forward and reverse channel bit rates and the number of bits required in the sample interval. The number of
347 bits required in the sample interval is based on the data precision required, the number of data sources and the
348 required safety-case capability.
- 349 4. The reverse communication channel bit rate can be defined by the system implementers within the limits
350 specified in Section 4.3. The overall system reverse communication channel bit rate must fall within the
351 capability of every device in the system.
- 352 5. The Data Link Layer can be defined by the system implementers within the limit specified in Section 5. The
353 Data Link Layer can be hard-coded at either the master or the slaves. If the Data Link Layer is hard-coded at
354 the master then all devices must support the same Data Link Layer. If the master supports a configurable Data
355 Link Layer, then slaves with different Data Link Layers can be supported in any combination within the
356 capability of the system.
- 357 6. Clock synchronization and timing optimization occurs at multiple levels and is considered a shared
358 responsibility among the devices in the system. Simple low speed system goals can be met with minimal clock
359 synchronization and no timing optimization. More complex high speed system goals can be met by utilizing
360 the temporal framework to optimize system timing, as described in Section 4.5. Devices of minimal capability
361 can be mixed with more capable devices on a bus however the system implementers must configure the timing
362 to account for the mix of capabilities. The theoretical maximum system capability will be compromised by the
363 less capable devices.
- 364 7. System fault tolerance and operability can be defined by the system implementers through both physical layer
365 configurations and Data Link Layer configurations. Fault detection and operability is a shared responsibility
366 between the master and slave(s). If desired, fault isolation can be implemented at the slaves through the use of
367 bus switches.

368 Parameters in this document marked with a “†” are scalable parameters. Scalable parameters include a controlling
369 dimension number from the above list as well as a parenthetic suggested value for typical systems.

370 The scalable parameter capability of devices in a system must be documented in the device datasheets to allow the
371 system implementer to determine the lowest common capability in each controlling dimension.

4 DSI3 Physical layer

372

4.1 Introduction

373

374 DSI3 defines a forward channel for master to slave communication and a reverse channel for slave to master
 375 communication. The forward channel uses voltage fluctuations and the reverse channel uses current fluctuations. DSI3
 376 uses a half-duplex command and response transaction model. With the command and response transaction model the
 377 master always initiates the communication cycle via a command.

378 The physical layer consists of a connection between a single master and one or multiple slaves. The physical layer
 379 interface provides both power and data communication signals. The bus topologies are defined in section 2.2.

380 The command and response transactions occur in sequence. The half-duplex command and response characteristic is
 381 shown in section 2.4 for both the Signal Function Class (Figure 2-4) and for the Power Function Class (Figure 2-7).

382 For the Periodic Data Collection Mode (Figure 2-5 and Figure 2-6), one or more slaves encode their data source(s)
 383 utilizing an optimized multi-level source coded TDMA method. The source coding encodes data nibbles into multi-
 384 level symbols. System timing optimizations are also possible through the use of the global clock synchronization, clock
 385 management and innovative response time assignment methods. These system timing optimizations are covered in
 386 Section 4.5.

4.2 Forward Communication Channel Physical Layer

387

388 Two modes of communication are defined. The Command and Response Mode is used for system configuration and
 389 for applications that require significant message traffic in both the forward and reverse directions. The Periodic Data
 390 Collection Mode is used for applications that require significant message traffic in only the reverse direction. The
 391 Background Diagnostic Mode allows for low speed bidirectional message traffic while preserving most of the
 392 bandwidth for high speed periodic data collection (reference Section 2.4.3).

393 The forward communication channel physical layer maximum ratings are listed in Table 4-1

| Item | Characteristic / Symbol | Condition / Notes | Max | Unit |
|------|----------------------------|-----------------------|--------------------------------|------|
| 1. | V _{IDLE} | Power Function Class | 25 | V |
| 2. | V _{HIGH} | Signal Function Class | 20 | V |
| 3. | Reverse Voltage Protection | Power Function Class | ⌈2 (-I _{CL_PWR_MAX}) | mA |
| 4. | Reverse Voltage Protection | Signal Function Class | ⌈2 (-I _{CL_SIG_MAX}) | mA |

394

Table 4-1: Forward Communication Physical Layer Maximum Ratings

395

396 4.2.1 Forward Channel Physical Layer - Master Perspective

397 4.2.1.1 Signal Function Class Forward Channel Physical Layer – Master Perspective

398 The V_{HIGH} and V_{LOW} voltages are required for all operational modes of the Signal Function Class.

399 The average value of the V_{HIGH} voltage is held constant and the V_{LOW} voltage is produced relative to V_{HIGH} such that
 400 V_{HIGH} minus V_{LOW} is equivalent to V_{DELTA} . For typical applications the master derives the V_{HIGH} and V_{LOW} voltages
 401 from an externally regulated voltage source with sufficient voltage and current capabilities.

402 The master is responsible for supplying power to the bus loads. The total bus load consists of static and dynamic loads.
 403 The static loads are the slave quiescent currents. The dynamic loads consist of the response currents and the bus
 404 currents required to charge and discharge the harness and load capacitors used for bus filtering and stabilization. The
 405 slave quiescent current is typically supplied by the master at either of the V_{HIGH} or V_{LOW} voltages. As an alternative for
 406 extreme low voltage applications the Signal Function Class slave could supply quiescent current from a backup
 407 capacitor while at the V_{LOW} voltage.

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|---|---|----------|-----|----------|----------|
| 5. | V_{HIGH} | Signal High Voltage | ⌚1 (3) | | 20 | V |
| 6. | V_{HIGH_pp} drift | Variation in V_{HIGH} Over 10ms Ignoring Effects of Signaling | -150 | | 150 | mV |
| 7. | R_M | Master Source Resistance | | | 10 | Ω |
| 8. | V_{HIGH_pp} During Response Phase | Measured at Master, Peak to Peak Response Current $\leq 27mA$ | -500 | | 500 | mV |
| 9. | $I_{CL_SIG_MAX}$ | Supply Voltage Current Limit, Measured at Master | ⌚2 (80) | | ⌚2 (100) | mA |
| 10. | V_{HIGH} Minus V_{LOW} Differential Signaling Voltage (V_{DELTA}) | Measured at Master, $I_Q \leq 40mA$ | 1.75 | 2 | 2.25 | V |
| 11. | V_{HIGH} to V_{LOW} Slew Time | $C_{BUS} = 15nF$, 90% to 10% of V_{DELTA} | ⌚2 (333) | | 1000 | ns |
| 12. | V_{LOW} to V_{HIGH} Slew Time | $C_{BUS} = 15nF$, 10% to 90% of V_{DELTA} | ⌚2 (333) | | 1000 | ns |

408 **Table 4-2: Signal Function Class Forward Channel Physical Layer Parameters**

409

410 4.2.1.2 Power Function Class Forward Channel Physical Layer – Master Perspective

411 The $V_{\text{HIGH-PWR}}$ and $V_{\text{LOW-PWR}}$ voltages are required for all operational modes of the Power Function Class. The V_{IDLE}
412 voltage is required for the power phase.

413 The $V_{\text{HIGH-PWR}}$ and $V_{\text{LOW-PWR}}$ voltages are used for communication only. $V_{\text{HIGH-PWR}}$ and $V_{\text{LOW-PWR}}$ are fixed voltages as
414 specified in Table 4-3.

415 The slave load current comes from a reservoir capacitor (H_{CAP}) during the command and response phase of the
416 communication cycle. The H_{CAP} is re-supplied during the power phase of the communication cycle. Current for the
417 Power Function Class loads is supplied from the master during the power phase. The flow of current between the
418 master and the H_{CAP} is controlled with a power extraction diode or by synchronous rectification with an active switch.

419 The total bus load consists of static and dynamic loads. The static loads are the slave quiescent currents and any
420 additional loads that do not vary significantly during the response phase. The dynamic loads consist of the response
421 currents, the currents to recharge the H_{CAP} and the bus currents required to charge and discharge the harness and load
422 capacitors used for bus filtering and stabilization.

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|---|--|-----------------------|-----|----------------------|----------|
| 13. | V_{IDLE} | Power Phase Idle Voltage | -- | | 25 | V |
| 14. | V_{IDLE} Minus $V_{\text{HIGH-PWR}}$ | Difference Between the Power Phase Idle Voltage and the Signal High Voltage | 1 | | | V |
| 15. | $V_{\text{HIGH-PWR}}$ | Power Function Class Signal High Voltage | 3.5 | 4 | 4.5 | V |
| 16. | $V_{\text{LOW-PWR}}$ | Power Function Class Signal Low Voltage | 1.75 | 2 | 2.25 | V |
| 17. | R_{M} | Master Source Resistance | | | 10 | Ω |
| 18. | $V_{\text{HIGH-PWR_PP}}$ During Response Phase | Measured at Master Peak to Peak Response Current $\leq 27\text{mA}$ | -500 | | 500 | mV |
| 19. | $I_{\text{CL_PWR_MAX}}$ | Supply Voltage Current Limit, Measured at Master | \updownarrow (200) | | \updownarrow (400) | mA |
| 20. | $V_{\text{HIGH-PWR}}$ to $V_{\text{LOW-PWR}}$ Slew Time | $C_{\text{BUS}} = 15\text{nF}$, 90% to 10% of V_{DELTA} | \updownarrow (333) | | 1000 | ns |
| 21. | $V_{\text{LOW-PWR}}$ to $V_{\text{HIGH-PWR}}$ Slew Time | $C_{\text{BUS}} = 15\text{nF}$, 10% to 90% of V_{DELTA} | \updownarrow (333) | | 1000 | ns |
| 22. | V_{IDLE} to $V_{\text{HIGH-PWR}}$ Slew Time | $C_{\text{BUS}} = 15\text{nF}$, 90% to 10% of $V_{\text{IDLE}} - V_{\text{HIGH-PWR}}$ | \updownarrow (1000) | | 8000 | ns |
| 23. | $V_{\text{HIGH-PWR}}$ to V_{IDLE} Slew Time | $C_{\text{BUS}} = 15\text{nF}$, 10% to 90% of $V_{\text{IDLE}} - V_{\text{HIGH-PWR}}$ | \updownarrow (1000) | | 8000 | ns |

423 **Table 4-3: Power Function Class Forward Channel Physical Layer Parameters**

424 4.2.2 Forward Channel Physical Layer - Slave Perspective

425 The slave must track the average value of the V_{HIGH} voltage. From the average V_{HIGH} voltage the slave can determine
426 the V_{LOW} voltage relative to the V_{HIGH} voltage.

427 The slave voltage regulation scheme must be designed to account for the V_{HIGH} and V_{LOW} voltage levels (line
428 regulation). For Power Function Class slaves the slave must also detect the V_{IDLE} voltage and isolate load currents
429 from the communication response current during the response phase.

430 The slave quiescent current must remain stable during the response phase. For Signal Function Class slaves a series
431 voltage regulation scheme can ensure stable quiescent current draw. For Power Function Class slaves the energy
432 extraction scheme isolates the slave load current from the response current during response phase.

433

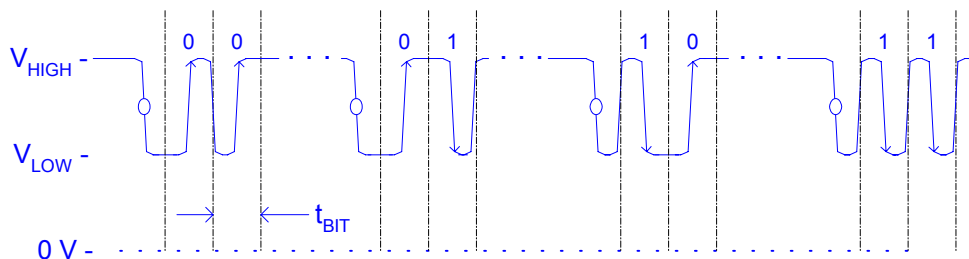
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434 4.2.3 Forward Communication Channel Data Bit Encoding

435 The master Manchester encodes forward channel data bits onto the bus as transitions between the V_{HIGH} and V_{LOW} bus
 436 voltages. For the Power Function Class, the transitions between the V_{IDLE} and the V_{HIGH_PWR} voltages do not encode
 437 any information.

438 4.2.3.1 Forward Channel Data Bit Encoding - Master Perspective

439 For Command and Response Mode the master directly encodes forward channel data bits using a Manchester-1 format
 440 where V_{HIGH} is considered the idle level and V_{LOW} is considered the signal level. Logic 1 bits are encoded as a
 441 transition from V_{HIGH} to V_{LOW} whereas logic 0 bits are encoded as a transition from V_{LOW} to V_{HIGH} as shown in Figure
 442 4-1.



443

444 **Figure 4-1: Forward Channel - Data Bit Encoding Examples**

445 For Command and Response Mode all commands begin with a transition from the V_{HIGH} voltage to the V_{LOW} voltage
 446 levels and this transition occurs as defined within the temporal framework. The initial transition is followed by the
 447 command bits as illustrated in Figure 4-1. The bit timing and tolerances are defined in Section 4.2.4.

448 For the Periodic Data Collection Mode the master sends a Broadcast Read Command. If the Background Diagnostic
 449 Mode is used, the Broadcast Read Command is replaced by a predetermined number of Manchester encoded bits that
 450 make up a complete diagnostic command over consecutive time periods. The number of diagnostic command bits sent
 451 during each successive time period is based on the amount of reverse channel bandwidth allocated to the Background
 452 Diagnostic Mode (reference Section 2.4.3).

453 The V_{HIGH} to V_{LOW} voltage levels for the forward channel are specified in Section 4.2.1. The timings parameters for the
 454 forward channel are specified in Section 4.2.4.

455 4.2.3.2 Forward Channel Data Bit Decoding ~ Slave Perspective

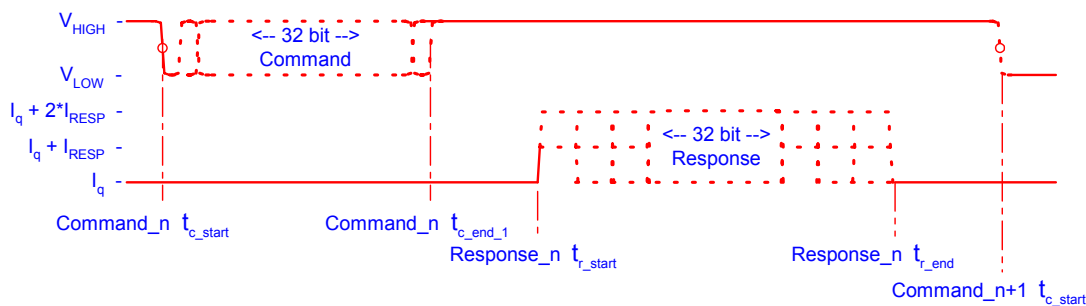
456 The slave must detect the transition and transition polarity between the V_{HIGH} and V_{LOW} voltage levels. Polarity
 457 discrimination is used for command decoding and for clock synchronization.

458

459 **4.2.4 Forward Communication Channel Timing**

460 Figure 4-2 shows the standard timing for a single Command and Response Mode transaction. For Command and
 461 Response Mode there are defined time delays between the command phase and the response phase. For Power
 462 Function Class, the master asserts the power phase following the command and response phase with an associated time
 463 delay. Timings for the Command and Response Mode are relative to the initial transition from V_{HIGH} to V_{LOW} and are
 464 preceded by a defined quiet time.

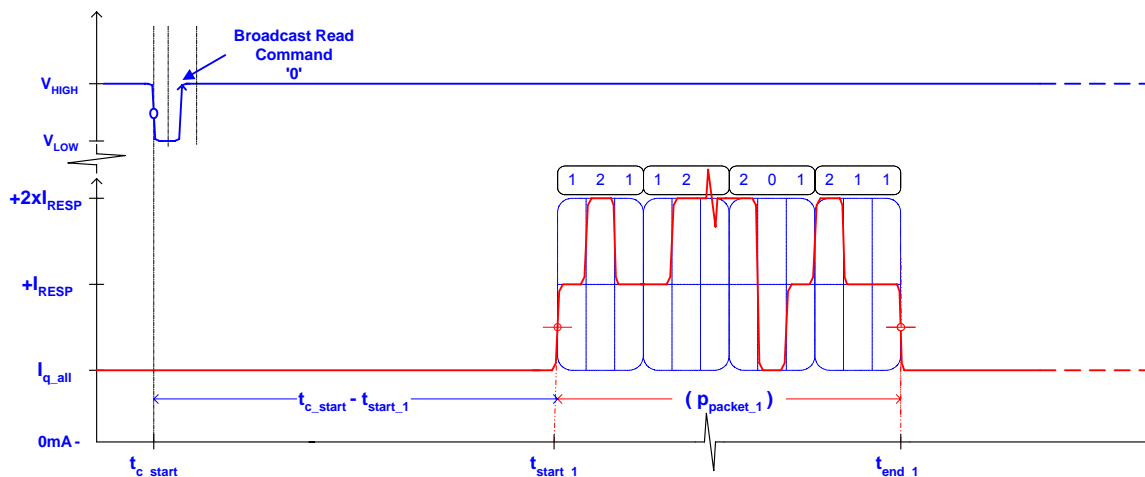
465 Section 4.5 introduces methods to take advantage of the protocol temporal framework to improve the system timing.
 466 Implicit start bits are not required.



467

468 **Figure 4-2: Command and Response Mode Transaction**

469 Figure 4-3 shows the standard timing for a single Periodic Data Collection Mode transaction. In the Periodic Data
 470 Collection Mode the initial V_{HIGH} to V_{LOW} transition occurs at a pre-defined period as required by the application and
 471 verified by the temporal framework. Implicit start bits are not required.



472

473 **Figure 4-3: Periodic Data Collection Mode Transaction**

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|------------------------------|----------------------------|--------------|-----|-------------|---------|
| 24. | t_{BIT_CRM} (Figure 4-1) | Command Bit Time in CRM | | 8 | | μs |
| 25. | t_{BIT_PDCM} (Figure 4-1) | Command Bit Time in PDCM | | 8 | | μs |
| 26. | t_{BIT_BDM} (Figure 4-1) | Command Bit Time in BDM | | 8 | | μs |
| 27. | t_{BIT_TOL} | Command Bit Time Tolerance | ± 6 (-1) | | ± 6 (1) | % |

474

Table 4-4: Forward Communication Timing Parameters

Implementation of the Bus Standard is governed by the terms of Section 1.3 of this document. Changes to this specification must be agreed to by DENSO CORPORATION, FREESCALE SEMICONDUCTOR INC. and TRW AUTOMOTIVE INC.

475 4.3 Reverse Communication Channel Physical Layer

476 The reverse communication physical layer is a current loop interface. There are three current levels defined for the
 477 reverse channel: the total quiescent current of all connected slaves (I_Q), the 1x response level (I_{RESP}) and the 2x
 478 response level ($2 \cdot I_{RESP}$).

479 4.3.1 Reverse Communication Channel Physical Layer - Slave Perspective

480

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|----------------------------|---|--------------------|-----|------|------|
| 28. | $2 \cdot I_{RESP}$ | Second Level Response Current During Response Phase Not Including I_Q | 21 | 24 | 27 | mA |
| 29. | I_{RESP} | First Level Response Current During Response Phase No Including I_Q | 10.5 | 12 | 13.5 | mA |
| 30. | Response Current Slew Time | 10% to 90% of $2 \cdot I_{RESP}$ | $\uparrow 4$ (200) | | 1000 | ns |

481 **Table 4-5: General Reverse Channel Physical Layer Slave Parameters**

482 For Signal Function Class slaves, the reverse channel response signal assumes 3 distinct values: I_Q , $I_Q + I_{RESP}$ and
 483 $I_Q + 2 \cdot I_{RESP}$. I_Q is the total quiescent current for all connected slaves. I_Q must remain stable over periods of time
 484 significantly longer than the message.

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|-------------------------|--|-----|-----|-------------------|------|
| 31. | I_Q | Total Static Bus Loading | | | $\uparrow 2$ (40) | mA |
| 32. | I_{q_Slave} | Static Bus Loading per Slave | | | $\uparrow 2$ (10) | mA |
| 33. | ΔI_Q | Change in Static Bus Loading Over Life | -5 | | 5 | mA |
| 34. | $d I_Q / dt$ | Total Static Bus Load Rate of Change During Response Phase Excluding Response Signal Current | | | 1 | mA/s |

485 **Table 4-6: Signal Function Class Reverse Channel Physical Layer Slave Parameters**

486 For Power Function Class slaves the reverse channel response signal assumes 3 distinct values: I_{Q_PWR} , $I_{Q_PWR} + I_{RESP}$
 487 and $I_{Q_PWR} + 2 \cdot I_{RESP}$. The load current and the response current are isolated from each other as described in Section
 488 2.4.4.

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|-------------------------|--|-----|-----|--------------------|------|
| 35. | I_{LOAD_PWR} | Total Bus Load in Idle Phase | | | $\uparrow 2$ (100) | mA |
| 36. | I_{Q_PWR} | Total Static Bus Loading During Communication Phase | | | 1 | mA |
| 37. | $d I_Q / dt$ | Total Static Bus Load Rate of Change During Response Phase Excluding Response Signal Current | | | 0.1 | mA/s |

489 **Table 4-7: Power Function Class Reverse Channel Physical Layer Slave Parameters**

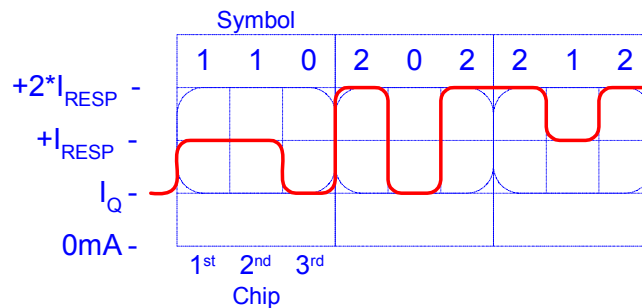
490 4.3.2 Reverse Communication Channel Physical Layer - Master Perspective

491 The master interface must dynamically monitor the current supplied to the bus. In particular the master must sample
 492 the current supplied to the bus with sufficient resolution and sample rate to detect and discriminate between the 3
 493 distinct currents. This detection and discrimination must assess both the magnitudes of the currents and the transitions
 494 between the various levels. Additionally the master must detect if the current is outside of the range appropriate for the
 495 slave class or if the magnitudes or transitions violate specific timing and magnitude criteria.

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4.3.3 Reverse Communication Channel Data Bit Encoding

DSI3 uses multi-level source coded approach where data nibbles are first encoded into symbols and then the symbols are encoded into current levels. Within a symbol there are 3 consecutive transmissions called *chips* that can assume one of the three discrete current levels described in Section 4.3. Each symbol encodes the information of 4-bits. Figure 4-4 shows an example of a 3 symbol (9-chip) data packet (12 data bits).



501

502 **Figure 4-4: Response Data Bit Encoding - "Multi-Level Source Coded"**

503 Of the 27 possible combinations for three consecutive tri-level chips, the combinations that begin with the null current
 504 level (I_Q) are discarded. Of the remaining 18 symbols, the two symbols that contain the same value for all three chips
 505 are also discarded. The remaining 16 symbols all begin with a non-null current level and have at least one transition.
 506 These characteristics guarantee that any response packet has a transition at the beginning of a packet and at least one
 507 transition in every symbol. Table 4-8 specifies the symbol encoding used for DSI3 response transmissions.

| Encoded Data (4-Bits) | | Symbol Transmitted | | |
|-----------------------|-------------|----------------------|----------------------|----------------------|
| Binary | Hexadecimal | 1 st Chip | 2 nd Chip | 3 rd Chip |
| 0000 | 0 | 1 | 1 | 0 |
| 0001 | 1 | 2 | 1 | 1 |
| 0010 | 2 | 1 | 0 | 2 |
| 0011 | 3 | 2 | 0 | 2 |
| 0100 | 4 | 1 | 0 | 0 |
| 0101 | 5 | 2 | 1 | 2 |
| 0110 | 6 | 1 | 1 | 2 |
| 0111 | 7 | 2 | 0 | 1 |
| 1000 | 8 | 2 | 2 | 0 |
| 1001 | 9 | 2 | 1 | 0 |
| 1010 | A | 1 | 2 | 2 |
| 1011 | B | 2 | 2 | 1 |
| 1100 | C | 1 | 2 | 0 |
| 1101 | D | 2 | 0 | 0 |
| 1110 | E | 1 | 0 | 1 |
| 1111 | F | 1 | 2 | 1 |

508 **Table 4-8: Symbol Mapping Example: Source ID 0x00**

509 The reverse communication chip and symbol timing parameters are specified in Section 4.4. The timing parameters are
 510 typically global for all response packets on a DSI3 network. However the specification only requires that the master
 511 and slave use the same chip timings. Slaves with different chip timings could exist on the same network if the master
 512 has this capability.

513 4.3.3.1 Reverse Communication Channel Data Bit Encoding - Slave Perspective

514 The slave encodes groups of 4 data bits into symbols. The chip timing for each specific slave and its master must
515 agree. The slave is responsible for encoding the timing information present in the symbols for recovery by the master.
516 The variations of chip times are actively controlled within the tolerances of the clock synchronization and management
517 scheme. Additional restrictions and requirements for slave response data encoding are specified in the data link layer
518 Section 5

519 4.3.3.2 Reverse Communication Channel Data Bit Decoding - Master Perspective

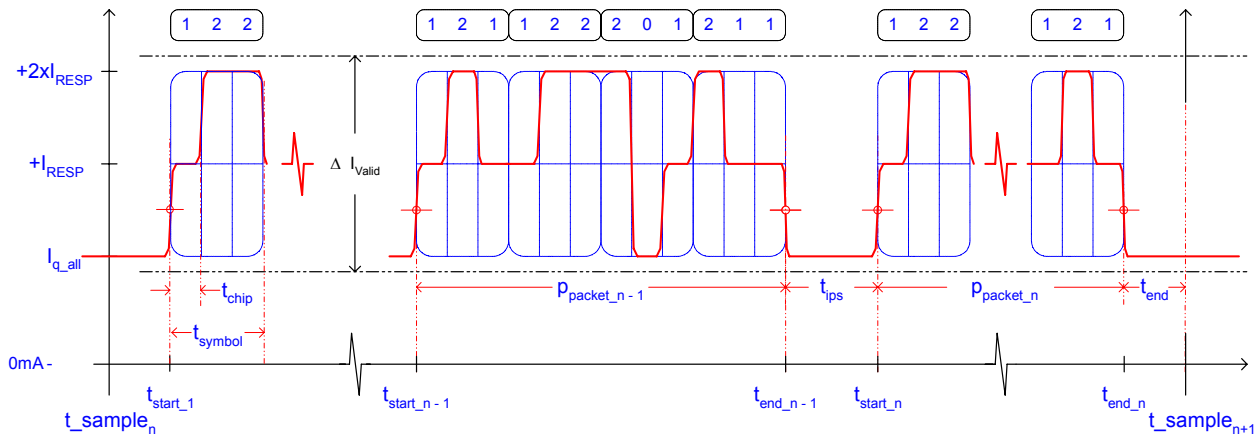
520 The master and slave must agree on a common chip time. The master synchronizes symbol recovery with the initial
521 transition that begins every response packet. Slave response symbols have at least one guaranteed transition, allowing
522 the master to re-synchronizes as necessary during symbol recovery. The master must ensure that the response current
523 levels are proper and that transitions between the specified levels occur at appropriate times. Finally each recovered
524 symbol must be one of the 16 possible symbols.

525

526 **4.4 Reverse Communication Channel Timing Considerations**

527 For the Periodic Data Collection Mode of the Signal Function Class multiple symbols are assembled into data packets
 528 and sent to the master as a TDMA frame. Figure 4-5 introduces the TDMA frame and some of the basic parameters
 529 associated with the frame. Each packet in the frame has a start time defined as a percentage of the sample period or in
 530 terms of real time. The time of the first packet is specified in terms of real time. The minimum or earliest time that the
 531 first packet can start allows sufficient time for a single bit command and the associated settling time. The first response
 532 packet in the TDMA frame may be further delayed based on the percentage of time reserved for Background
 533 Diagnostic Mode.

534 Section 4.5 introduces methods to take advantage of the protocol temporal framework to improve the system timing.



535

536 **Figure 4-5: Multi-Level Source Coded TDMA Response Frame**

537

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|-------------------------------|--|---------------------|----------------|---------------------|---------|
| 38. | t_{chip} Valid Range | Range of Valid Chip Times | $\uparrow 4$ (2.70) | | $\uparrow 4$ (10.0) | μs |
| 39. | t_{chip} Tolerance | Slave Chip Time Tolerance | -5.0 | | 5.0 | % |
| 40. | t_{symbol} | Symbol Time | | $3 * t_{chip}$ | | μs |
| 41. | $t_{r_start} - t_{e_start}$ | Response Start Time, CRM (Figure 4-2) | 280 | 295 | 310 | μs |
| 42. | $t_{start_1} - t_{e_start}$ | Response Start time, PDCM (Figure 4-3) | 15 | | | μs |
| 43. | t_{ips} | Inter-Packet Separation (Figure 3-5) | 1 | | | Chips |
| 44. | t_{END} | Quiet Time Before Next Sample Period | $\uparrow 6$ (10) | | | μs |

538

Table 4-9 : Reverse Communication Channel Timing Parameters

539

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540 4.5 System Timing Considerations

541 DSI3 defines a temporal framework and provides services for clock management and clock synchronization. The
 542 temporal framework enables the system to perform timing checks based on a common expectation of when events
 543 should occur within the system. The temporal framework allows the system to validate changes of state including the
 544 ordering of events within the changes of state. With the temporal framework all devices on a bus develop a common
 545 sense of time. Clock management and clock synchronization can be used to improve the efficiency of the system.
 546 Commands define a *base period* for Periodic Data Collection Mode and perform basic clock synchronization. The
 547 temporal framework provides error checks and validates the expected timing of the synchronization events.

548 The master node transmits commands at P_{SYS} period from a stable time base of sufficient accuracy. The accuracy of the
 549 system generated synchronization period ΔP_{SYS} is inherited by the master ΔP_{Master} and then by the slave node ΔP_{Slave} .
 550 The system period variation ΔP_{SYS} limits the overall accuracy of the system.

551 Clock management at slave nodes is based on the number of local oscillator cycles counted between commands. The
 552 slave can also actively manage the local oscillator period to maintain the number of local oscillator cycles between
 553 commands constant. Finally all of the timings in Periodic Data Collection Mode can be defined as fractional units of
 554 the base period.

555 Table 4-10 shows an example set of system parameters using the temporal framework to improve system timing. These
 556 parameters are not required by the standard, but are only included as an example to show the potential of the temporal
 557 framework to improve system timing.

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|----------------------------------|--|------|-----|------|----------------|
| 45. | P_{SYS} | Range of Valid PDCM Periods, Example, not an Absolute Specification | 100 | | 5000 | μs |
| 46. | ΔP_{SYS} | PDCM Period Tolerance at the Master, Example, not an Absolute Specification | | | 200 | ppm |
| 47. | ΔP_{Master} | Master PDCM Period Tolerance, Example, not an Absolute Specification | -0.1 | | 0.1 | % P_{SYS} |
| 48. | ΔP_{Slave} | Measured PDCM Period at the Slave, Example, not an Absolute Specification | -0.7 | | 0.7 | % P_{Master} |
| 49. | $\Delta f_{Osc_Slave_Trained}$ | Trained Slave Oscillator Tolerance, Example, not an Absolute Specification | -0.5 | | 0.5 | % |
| 50. | Δt_{Period} | PDCM Sample Period Jitter, Example, not an Absolute Specification | -0.1 | | 0.1 | % P_{Master} |

558 **Table 4-10: Example of DSI3 Timing Parameters Utilizing the Temporal Framework**

559

560 **4.6 Number of DSI Buses and Nodes**

561 A DSI3 bus consists of single master and one or more slaves. The terms “network” and “bus” are used interchangeably
562 with additional specificity concerning topology and class. DSI3 defines no maximum limit to the number of busses
563 (networks) allowed in a system.

564 The maximum number of nodes on a DSI bus is 16 (1 master and 15 slaves). The minimum number is 2 (1 master and
565 1 slave). Each Signal Function Class slave supplies one or more data sources. Each Power Function Class slave
566 supplies one or more power outputs and signal sources required for the intended function.

567 **4.7 Class-Mix and Mode Restrictions and Number of Nodes**

568 Signal Function Class slaves can operate on the same bus with Power Function Class slaves provided that the master
569 accounts for the quiescent current of the Signal Function Class slaves. Also the Signal Function Class slave must
570 tolerate the idle voltage of the Power Function Class. Power Function Class slaves cannot exist on a Signal Function
571 Class bus since there is no power phase.

572 Signal Function Class and Power Function Class slaves both support the Command and Response Mode. The Signal
573 Function Class also supports the Periodic Data Collection Mode and, optionally, the Background Diagnostic Mode.

574

5 DSI3 Data Link Layer

575 5.1 Introduction

576 The general philosophy of the DSI-3 data link layer follows earlier versions of the DSI specification in the sense that
577 there is sufficient flexibility to tailor the protocol to satisfy the needs of diverse applications. This section is concerned
578 primarily with the three fundamental modes of operation for the Signal Function Class: the Command and Response
579 Mode, the Periodic Data Collection Mode and the Background Diagnostic Mode, as well as the Command and
580 Response Mode for the Power Function Class.

581 For the Command and Response Mode a single command packet is followed by at most one response packet (There is
582 no response packet for a global command).

583 For the Periodic Data Collection Mode a command packet is followed by multiple response packets separated by inter-
584 packet separation times following a TDMA philosophy. The command packets for the Periodic Data Collection Mode
585 are strictly periodic. The DSI3 standard does not limit the maximum number of response packets or the lengths of the
586 response packets for Periodic Data Collection Mode. The master implementation imposes the practical limits on the
587 maximum number and lengths of the response packets. The Periodic Data Collection Mode response packet start
588 positions and lengths must be configured before entering Periodic Data Collection Mode. A preconfigured system can
589 transition into Periodic Data Collection Mode immediately after applying power to the bus.

590 5.1.1 Command Message Bit Order

591 Most significant bits/bytes are transmitted before least significant bits/bytes. This ordering applies to both the message
592 bits and the CRC bits. Messages bits are transmitted before the CRC bits. This ordering allows for in-line CRC serial
593 calculations that terminate in an all zero value for successful transfers.

594 5.1.2 Response Message Bit Order

595 Most significant bits/bytes are transmitted before least significant bits/bytes. This ordering applies to both the message
596 bits and the CRC bits. Messages bits are transmitted before the CRC bits. This ordering allows for in-line CRC serial
597 calculations that terminate in an all zero value for successful transfers.

598

5.2 Signal Function Class

5.2.1 Command and Response Mode Packet Formats

Command and Response Mode data packets are exchanged primarily between a single master and a single slave. The one exception to this is the use a global command which can be transmitted from one master to multiple slaves but includes no slave response. The primary purpose of the command and response transactions are to read from and to write to registers within the slave memory. Command and Response Mode utilizes a memory mapped access philosophy to interface with slave registers. By changing the contents of slave data registers the application can read, write or verify configuration of the slave and effect changes of state within the slave. The command, address and data based interface used in previous versions of the protocol are also available. The system implementer may choose between the memory mapped register access method and the command, address and data method. However the memory mapped method provides greater flexibility.

The command and response structure provides all of the context information required for unambiguous single-exchange transactions for extended memory applications requiring safety critical and efficient memory access. The structures have pre-defined fixed bit timings for both the command and response packets. The transactions for the Signal Function Class are intended to be periodic and this feature may be used for initial clock training and temporal frame work initialization as described in Section 4.5. The standard defines a set of fields that constitute the command and response message structure. The details of the command formats can be preprogrammed within the implementation or configured at run-time.

The Command and Response Mode command format is shown in Table 5-1.

| MSB | | | | LSB |
|------------------|----------|---------------|---------------|----------|
| Physical Address | Command | Extended Data | Register Data | CRC |
| PA[3:0] | CMD[3:0] | ED[7:0] | RD[7:0] | CRC[7:0] |

Table 5-1: Command and Response Mode - Command Format

The Command and Response Mode response format is shown in Table 5-2.

| MSB | | | | LSB |
|------------------|--------|---------------|---------------|----------|
| Physical Address | Status | Extended Data | Register Data | CRC |
| PA[3:0] | S[3:0] | ED[7:0] | RD[7:0] | CRC[7:0] |

Table 5-2: Command and Response Mode - Response Format

The field definitions are shown in Table 5-3.

| Field | Command Packet | Length (Bits) | Field | Response Packet | Length (Bits) |
|----------|------------------|---------------|----------|------------------|---------------|
| PA[3:0] | Physical Address | 4 | PA[3:0] | Physical Address | 4 |
| CMD[3:0] | Command | 4 | S[3:0] | Status | 4 |
| ED[7:0] | Extended Data | 8 | ED[7:0] | Extended Data | 8 |
| RD[7:0] | Register Data | 8 | RD[7:0] | Register Data | 8 |
| CRC[7:0] | | 8 | CRC[7:0] | | 8 |

Table 5-3: Command and Response Mode - Field Definitions

624 The Command and Response Mode supports the commands listed in Table 5-4:

| Command | Command Description | Extended Data ED[7:0] |
|---------|--------------------------|--------------------------|
| 0 | Register Read | Register Address RA[7:0] |
| 2 – 7 | Device / System Specific | Device / System Specific |
| 8 | Register Write | Register Address RA[7:0] |
| 9 - 15 | Device / System Specific | Device / System Specific |

625 **Table 5-4: Command and Response Mode - Supported Commands**

626 The Signal Function Class Command and Response Mode response status is defined in Table 5-5, with an example
627 implementation:

| Commands 0 and 8 | | | |
|---------------------------------------|--------|-----------------------|--------------------------------------|
| S[3] | S[2:0] | Standard Description | Device Description (Example) |
| Command Echo | 0 | Normal Mode | Normal Mode |
| | 1 | Exception Condition 1 | Self Test Active – Channel 1, Mode 1 |
| | 2 | Exception Condition 2 | Self Test Active – Channel 1, Mode 2 |
| | 3 | Exception Condition 3 | Self Test Active – Channel 1, Mode 3 |
| | 4 | Exception Condition 4 | Self Test Active – Channel 2, Mode 1 |
| | 5 | Exception Condition 5 | Self Test Active – Channel 2, Mode 2 |
| | 6 | Exception Condition 6 | Self Test Active – Channel 2, Mode 3 |
| | 7 | Exception Condition 7 | Internal Error |
| Commands 1 through 7 and 9 through 15 | | | |
| Command Echo | | | |

628 **Table 5-5: Signal Function Class Command and Response Mode - Status Definitions**

629

630 5.2.2 Periodic Data Collection Mode Packet Formats

631 In order to maximize system flexibility, the transition from Command and Response Mode to Periodic Data Collection
632 Mode is managed by the system implementer and not covered by this standard. Three example transition methods are
633 described below:

- 634 1. A Special Global DSI Command and Response Mode command can be implemented to simultaneously
635 transition all slaves from Command and Response Mode to Periodic Data Collection Mode.
- 636 2. A normal Command and Response Mode register write can be transmitted to each slave individually to
637 transition the slave to Periodic Data Collection Mode.
- 638 3. All slaves automatically transition from Command and Response Mode to Period Data Collection Mode based
639 on the master command message type.

640 Periodic Data Collection Mode response data packets are transferred from one or multiple slaves to a single master.
641 The primary purpose of Periodic Data Collection Mode transactions is to transfer high speed synchronous data from
642 multiple data sources. Slaves transmit data upon receiving a Broadcast Read Command or a Background Diagnostic
643 Mode command packet using the TDMA approach described in Section 2.4.2.

644 Slaves may include multiple data sources and may have varying data lengths. For this reason, the field lengths for
645 Periodic Data Collection Mode are variable. The field lengths are typically global for all slaves on the DSI3 network.
646 However this specification only requires that the master and slave agree on the field lengths. Slaves with different field
647 lengths could exist on the same network if the master has this capability. The field lengths are bounded by the values
648 listed below.

649

650 The Periodic Data Collection Mode response format is shown in Table 5-6:

| MSB | | | | LSB | | | | |
|------------|------------|--------------------|------------|------------|------------|------------|------------|----------|
| Source ID | | Keep Alive Counter | | Status | | Data | | CRC |
| SI[x:0] | | KAC[x:0] | | S[x:0] | | RD[x:0] | | CRC[7:0] |
| Min (Bits) | Max (Bits) | Min (Bits) | Max (Bits) | Min (Bits) | Max (Bits) | Min (Bits) | Max (Bits) | (Bits) |
| 0 | 8 | 0 | 4 | 0 | 4 | 8 | -- | 8 |

651 **Table 5-6: Periodic Data Collection Mode - Response Format**

652 **5.2.2.1 Source ID (SI)**

653 The source identifier field includes a logical address for the data source. The Source identifier can be the same as the
 654 physical address or a unique identifier. The source identifier can be pre-programmed, or assigned using Command and
 655 Response Mode after a physical address is assigned as described in Section 6.3. The Source ID field size is system
 656 configurable from 0 (no source identifier included) to 8 bits.

657 **5.2.2.2 Keep Alive Counter (KAC)**

658 The Keep Alive Counter (KAC) field is a free running rollover counter which is incremented after every message
 659 transmitted from a slave. The purpose of the KAC is to identify if a message transmission is skipped, or to identify loss
 660 of message synchronization between the master and a slave. The KAC counter size is system configurable from 0 (no
 661 counter) to 4 bits.

662 **5.2.2.3 Status (S)**

663 The status field contains device status information specific to the slave. The status field size is system configurable
 664 from 0 (no status) to 4 bits. The status field contents are system configurable.

665 **5.2.2.4 Data (RD)**

666 The data field includes the periodic data to be transmitted from the slave. The data field size and contents are system
 667 configurable. The maximum data field size is not limited by this specification, only by the practical limits of the
 668 system. The data field contents are typically exclusively sensor data. However, this field is not restricted to sensor data
 669 only. It can also include status information, error information or other specific slave identification information.

670

671 5.2.3 Background Diagnostic Mode Packet Formats

672 Background Diagnostic Mode Command and Response Mode data packets are exchanged between a single master and
 673 a single slave. The primary purpose of Background Diagnostic Mode transactions are to verify status of slaves via
 674 register reads. Secondly, the Background Diagnostic Mode may also be used to change the state of a slave via
 675 register writes.

676 The Background Diagnostic Mode command format is shown in Table 5-7.

| MSB | | | | LSB |
|------------------|----------|---------------|---------------|----------|
| Physical Address | Command | Extended Data | Register Data | CRC |
| PA[3:0] | CMD[3:0] | ED[7:0] | RD[7:0] | CRC[7:0] |

677 **Table 5-7: Background Diagnostic Mode - Command Format**

678 The Background Diagnostic Mode response format is shown in Table 5-8.

| MSB | | | | LSB |
|------------------|--------|---------------|---------------|----------|
| Physical Address | Status | Extended Data | Register Data | CRC |
| PA[3:0] | S[3:0] | ED[7:0] | RD[7:0] | CRC[7:0] |

679 **Table 5-8: Background Diagnostic Mode - Response Format**

680 The field definitions are shown in Table 5-9.

| Field | Command Packet | Length (Bits) | Field | Response Packet | Length (Bits) |
|----------|------------------|---------------|----------|------------------|---------------|
| PA[3:0] | Physical Address | 4 | PA[3:0] | Physical Address | 4 |
| CMD[3:0] | Command | 4 | S[3:0] | Status | 4 |
| ED[7:0] | Extended Data | 8 | ED[7:0] | Extended Data | 8 |
| RD[7:0] | Register Data | 8 | RD[7:0] | Register Data | 8 |
| CRC[7:0] | | 8 | CRC[7:0] | | 8 |

681 **Table 5-9: Background Diagnostic Mode - Field Definitions**

682 The Background Diagnostic Mode supports the commands listed in Table 5-10:

| Command | Command Description | Extended Data ED[7:0] |
|---------|--------------------------|--------------------------|
| 0 | Register Read | Register Address RA[7:0] |
| 2 - 7 | Device / System Specific | Device / System Specific |
| 8 | Register Write | Register Address RA[7:0] |
| 9 - 15 | Device / System Specific | Device / System Specific |

683 **Table 5-10: Background Diagnostic Mode - Supported Commands**

684

685 Background Diagnostic Mode response status is defined in Table 5-11, with an example implementation:

| Commands 0 and 8 | | | |
|---------------------------------------|--------|-----------------------|--------------------------------------|
| S[3] | S[2:0] | Standard Description | Device Description (example) |
| Command Echo | 0 | Normal Mode | Normal Mode |
| | 1 | Exception Condition 1 | Self Test Active – Channel 1, Mode 1 |
| | 2 | Exception Condition 2 | Self Test Active – Channel 1, Mode 2 |
| | 3 | Exception Condition 3 | Self Test Active – Channel 1, Mode 3 |
| | 4 | Exception Condition 4 | Self Test Active – Channel 2, Mode 1 |
| | 5 | Exception Condition 5 | Self Test Active – Channel 2, Mode 2 |
| | 6 | Exception Condition 6 | Self Test Active – Channel 2, Mode 3 |
| | 7 | Exception Condition 7 | Internal Error |
| Commands 1 through 7 and 9 through 15 | | | |
| Command Echo | | | |

686

Table 5-11: Background Diagnostic Mode - Status Definitions

687

688 5.3 Power Function Class Transactions

689 The Power Function Class uses Command and Response Mode exclusively. Data packets are exchanged primarily
 690 between a single master and a single slave. The one exception to this is the use a global command which can be
 691 transmitted from one master to multiple slaves but includes no slave response. The primary purpose of the command
 692 and response transactions are to read from and write to registers within the slave memory. Command and Response
 693 Mode utilizes a memory mapped access philosophy to interface with slave registers. By changing the contents of slave
 694 data registers the application can read, write or verify configuration of the slave and effect changes of state within the
 695 slave. The command, address and data based interface used in previous versions of the protocol are also available. The
 696 system implementer may choose between the memory mapped register access method and the command, address and
 697 data method. However the memory mapped method provides greater flexibility.

698 The command and response structure provides all of the context information required for unambiguous single-exchange
 699 transactions for extended memory applications requiring safety critical and efficient memory access. The structures
 700 have pre-defined fixed bit timings for both the command and response packets. The standard defines a set of fields that
 701 constitute the command and response message structures. The details of the command formats can be preprogrammed
 702 within the implementation or configured at run-time.

703 The Power Function Class Command and Response Mode command format is shown in Table 5-12.

| MSB | | | | | LSB |
|------------------|----------|---------------|---------------|----------|-----|
| Physical Address | Command | Extended Data | Register Data | CRC | |
| PA[3:0] | CMD[3:0] | ED[7:0] | RD[7:0] | CRC[7:0] | |

704 **Table 5-12: Power Function Class Command and Response Mode - Command Format**

705 The Power Function Class Command and Response Mode response format is shown in Table 5-13.

| MSB | | | | | LSB |
|------------------|--------|---------------|---------------|----------|-----|
| Physical Address | Status | Extended Data | Register Data | CRC | |
| PA[3:0] | S[3:0] | ED[7:0] | RD[7:0] | CRC[7:0] | |

706 **Table 5-13: Power Function Class Command and Response Mode - Response Format**

707 The field definitions are shown in Table 5-14.

| Field | Command Packet | Length (Bits) | Field | Response Packet | Length (Bits) |
|----------|------------------|---------------|----------|------------------|---------------|
| PA[3:0] | Physical Address | 4 | PA[3:0] | Physical Address | 4 |
| CMD[3:0] | Command | 4 | S[3:0] | Status | 4 |
| ED[7:0] | Extended Data | 8 | ED[7:0] | Extended Data | 8 |
| RD[7:0] | Register Data | 8 | RD[7:0] | Register Data | 8 |
| CRC[7:0] | | 8 | CRC[7:0] | | 8 |

708 **Table 5-14: Power Function Class Command and Response Mode - Field Definitions**

709

710 The Power Function Class Command and Response Mode supports the commands listed in Table 5-15.

| Command | Command Description | Extended Data ED[7:0] |
|---------|--------------------------|--------------------------|
| 0 | Register Read | Register Address RA[7:0] |
| 2 – 7 | Device / System Specific | Device / System Specific |
| 8 | Register Write | Register Address RA[7:0] |
| 9 - 15 | Device / System Specific | Device / System Specific |

711 **Table 5-15: Power Function Class Command and Response Mode - Supported Commands**

712 The Power Function Class Command and Response Mode response status is defined in Table 5-16, with an example
713 implementation:

| Commands 0 and 8 | | | |
|---------------------------------------|--------|-----------------------|------------------------------|
| S[3] | S[2:0] | Standard Description | Device Description (Example) |
| Command Echo | 0 | Normal Mode | Normal Mode |
| | 1 | Exception Condition 1 | Actuator 1 State |
| | 2 | Exception Condition 2 | Actuator 2 State |
| | 3 | Exception Condition 3 | Actuator 3 State |
| | 4 | Exception Condition 4 | Actuator 4 State |
| | 5 | Exception Condition 5 | Actuator 5 State |
| | 6 | Exception Condition 6 | Actuator 6 State |
| | 7 | Exception Condition 7 | Internal Error |
| Commands 1 through 7 and 9 through 15 | | | |
| Command Echo | | | |

714 **Table 5-16: Power Function Class Command and Response Mode - Status Definitions**

715

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716 5.4 Error Checking

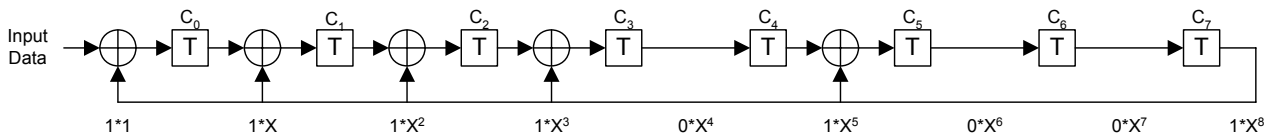
717 The master and slaves calculate a CRC on the entire message using the processes detailed below.

718 5.4.1 Command and Response Mode CRC

719 5.4.1.1 Command and Response Mode – Command CRC

720 The Command and Response Mode Command CRC is fixed at 8-bits in length for both Signal Function Class and
721 Power Function Class. It is calculated using the polynomial $x^8 + x^5 + x^3 + x^2 + x + 1$ with a seed value of binary
722 '11111111'.

723 An example CRC encoding implementation is shown in Figure 5-1.



724

726 **Figure 5-1: Command and Response Mode - Example CRC Encoder**

727 The CRC encoding procedure is listed below:

- 728 1. The seed value is preset into the least significant bits of the shift register.
- 729 2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least
730 significant bits of the shift register, MSB first.
- 731 3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length
732 of the CRC.
- 733 4. When the last zero is fed into the input adder, the shift register contains the CRC.
- 734 5. The CRC is transmitted.

735

736 The CRC decoding procedure is listed below:

- 737 1. The seed value is preset into the least significant bits of the shift register.
- 738 2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least
739 significant bits of the shift register in the order received (MSB first).
- 740 3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the
741 CRC check result.
 - 742 a. If the shift register contains all zeros, the CRC is correct.
 - 743 b. If the shift register contains a value other than zero, the CRC is incorrect.

744

745 Table 5-17 includes some example CRC calculations for Command and Response Mode commands.

| Physical Address (Hex) | Command (Hex) | Extended Data (Hex) | Register Data (Hex) | 8-Bit CRC (Hex) |
|------------------------|---------------|---------------------|---------------------|-----------------|
| 0x01 | 0x08 | 0x11 | 0x86 | 0xB0 |
| 0x02 | 0x01 | 0x25 | 0xFF | 0x38 |
| 0x03 | 0x0F | 0x1A | 0x41 | 0x2C |
| 0x04 | 0x01 | 0x01 | 0x01 | 0xD4 |

746 **Table 5-17: Command and Response Mode – Command CRC Calculation Examples**

747

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748 **5.4.1.2 Command and Response Mode – Response CRC**749 The Command and Response Mode response CRC is fixed at 8-bits in length for both Signal Function Class and Power
750 Function Class. It is calculated using the polynomial $x^8 + x^5 + x^3 + x^2 + x + 1$ with a seed value of binary '11111111'.751 The CRC encoding and decoding procedures are the same as the procedures for the Command and Response Mode
752 command CRC documented in section 5.4.1.1.

753 Table 5-18 includes some example CRC calculations for Command and Response Mode responses.

| Physical Address (Hex) | Status (Hex) | Extended Data (Hex) | Register Data (Hex) | 8-Bit CRC (Hex) |
|------------------------|--------------|---------------------|---------------------|-----------------|
| 0x01 | 0x09 | 0x11 | 0x86 | 0xBE |
| 0x02 | 0x09 | 0x25 | 0xFF | 0x48 |
| 0x03 | 0x09 | 0x1A | 0x41 | 0x08 |
| 0x04 | 0x09 | 0x01 | 0x01 | 0xA4 |

754 **Table 5-18: Command and Response Mode – Response CRC Calculation Examples**
755

756 5.4.2 Periodic Data Collection Mode CRC

757 The Periodic Data Collection Mode Response CRC is fixed at 8-bits in length. It is calculated using the polynomial
 758 $x^8 + x^5 + x^3 + x^2 + x + 1$. The seed value is determined using the Source ID as show in the following equation:

$$759 \text{Seed}_{CRC8} = \text{SourceID}[7:0]$$

760 The CRC encoding and decoding procedures are the same as the procedures for the Command and Response Mode
 761 command CRC documented in section 5.4.1.1.

762 Table 5-19 includes some example CRC calculations for Periodic Data Collection Mode responses.

| 8-Bit Source ID (Hex) | 4-Bit Keep Alive Counter (Hex) | 4-Bit Status (Hex) | 8-Bit Data (Hex) | 8-Bit CRC (Hex) |
|-----------------------|--------------------------------|--------------------|------------------|-----------------|
| 0x01 | 0x8 | 0x1 | 0x23 | 0x57 |
| 0x02 | 0x1 | 0x1 | 0x55 | 0x4E |
| 0x03 | 0xF | 0x1 | 0xAA | 0x6E |
| 0x04 | 0xC | 0x1 | 0xCE | 0x78 |
| 4-Bit (Hex) | 2-Bit (Hex) | 4-Bit (Hex) | 10-Bit (Hex) | 8-Bit (Hex) |
| 0x01 | 0x3 | 0x0 | 0x1FF | 0xD6 |
| 0x02 | 0x2 | 0x0 | 0x1FE | 0x70 |
| 0x03 | 0x1 | 0x0 | 0x20D | 0xB0 |
| 0x04 | 0x0 | 0x0 | 0x1EA | 0x5F |

763 **Table 5-19: Periodic Data Collection Mode – Response CRC Calculation Examples**

764 5.4.3 Background Diagnostic Mode CRC

765 5.4.3.1 Background Diagnostic Mode – Command CRC

766 The Background Diagnostic Mode Command CRC is fixed at 8-bits in length. It is calculated using the polynomial
 767 $x^8 + x^5 + x^3 + x^2 + x + 1$ with a seed value of binary ‘11111111’.

768 The CRC encoding and decoding procedures are the same as the procedures for the Command and Response Mode
 769 command CRC documented in section 5.4.1.1.

770 5.4.3.2 Background Diagnostic Mode – Response CRC

771 The Background Diagnostic Mode response CRC is fixed at 8-bits in length. It is calculated using the polynomial
 772 $x^8 + x^5 + x^3 + x^2 + x + 1$ with a seed value of binary ‘11111111’.

773 The CRC encoding and decoding procedures are the same as the procedures for the Command and Response Mode
 774 command CRC documented in section 5.4.1.1.

775

6 DSI3 Addressing

6.1 Introduction

777 DSI3 uses a combination of physical and source identification addresses. Physical addresses are required for every
 778 physical slave on a bus. A physical address can be augmented with a single or multiple source identification addresses.
 779 This section establishes a method for physical addressing and programming slave addresses in the system.

6.2 Physical Addressing for Slaves

781 Each slave device on the bus must have a unique 4-bit physical address. The physical address may be pre-programmed
 782 into the device or assigned automatically by the address assignment methods described in section 6.3.

783 Address 0 is reserved as a global address and is used for global commands. When using the global address the
 784 command phase is generally not followed by response phase. In the absence of a physical response, the slaves typically
 785 perform some action as a result of the global command. The device address encoding is shown in Figure 5-1.

| PA3 | PA2 | PA1 | PA0 | Slave Number |
|-----|-----|-----|-----|--------------|
| 0 | 0 | 0 | 0 | All Slaves |
| 0 | 0 | 0 | 1 | Slave 1 |
| 0 | 0 | 1 | 0 | Slave 2 |
| 0 | 0 | 1 | 1 | Slave 3 |
| 0 | 1 | 0 | 0 | Slave 4 |
| 0 | 1 | 0 | 1 | Slave 5 |
| 0 | 1 | 1 | 0 | Slave 6 |
| 0 | 1 | 1 | 1 | Slave 7 |
| 1 | 0 | 0 | 0 | Slave 8 |
| 1 | 0 | 0 | 1 | Slave 9 |
| 1 | 0 | 1 | 0 | Slave 10 |
| 1 | 0 | 1 | 1 | Slave 11 |
| 1 | 1 | 0 | 0 | Slave 12 |
| 1 | 1 | 0 | 1 | Slave 13 |
| 1 | 1 | 1 | 0 | Slave 14 |
| 1 | 1 | 1 | 1 | Slave 15 |

786

Table 6-1: Slave Address Encoding

787

788 **6.3 Address Assignment Methods**

789 The method used to obtain the physical address is determined based on the bus segment type. The sections below
790 describe these methods. Devices with pre-programmed physical addresses begin with the highest available address for
791 the segment and count down. Devices with un-programmed physical addresses can use any remaining available
792 address provided that they comply with the restrictions stated in the address assignment methods below.

793 **6.3.1 Address Assignment Method for Parallel Connected Slaves**

794 Parallel connected slaves must have unique, pre-programmed address. These devices do not participate in any address
795 assignment method. The identity and existence of parallel connected slaves must be known in advance.

796 **6.3.2 Address Assignment Method for Bus Switch Connected Daisy Chain Devices**

797 A bus switch connected daisy chain device may have either a pre-programmed, or an un-programmed address. It must
798 contain a high side bus switch which can connect the Bus High voltage to additional devices on the bus. A bus switch
799 connected daisy chain device with an un-programmed address must be the only device with an un-programmed address
800 on its bus segment. On power up, the bus switch connected daisy chain device must have its bus switch open.

801 Once power is applied to a bus switch connected device, it is the only device on the segment which requires an address
802 assignment. Using Command and Response Mode, the bus master transmits a global write command to assign the
803 physical address to the device. Once a physical address is assigned to the device, Command and Response Mode is
804 used with the assigned physical address to read device type information and to configure the device. This includes
805 closing the bus switch to connect the next device and/or bus segment to the master.

806

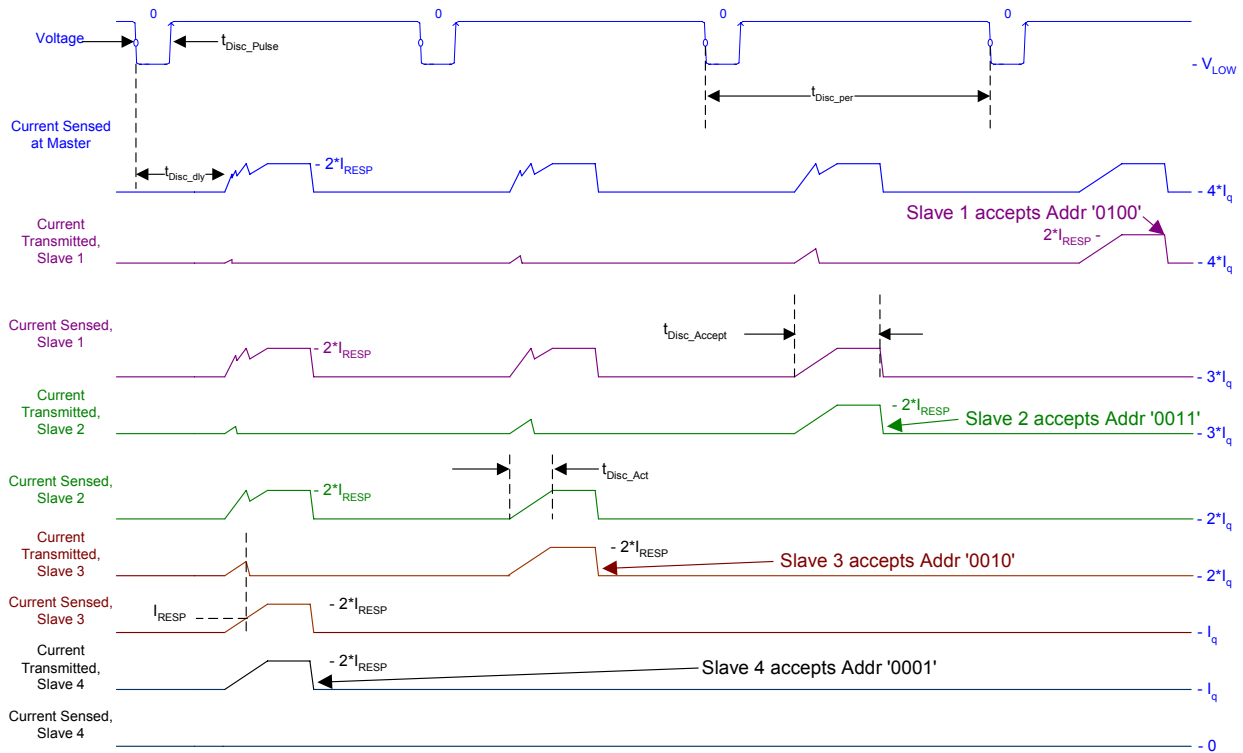
807 6.3.3 Address Assignment Method for Resistor Connected Daisy Chain Devices

808 A resistor connected daisy chain device has an un-programmed address. An address assignment method called
809 Discovery Mode is used to assign a physical address to each resistor connected daisy chain device on a bus segment.

810 Discovery Mode runs automatically after power is applied to the bus segment. The discovery time period begins
811 $t_{\text{Disc_Start}}$ after power is applied to the bus segment and requires $t_{\text{Disc_Per}}$ for every resistor connected daisy chain device on
812 the bus segment. Once Discovery Mode is complete, the master reads type information from each device using
813 Command and Response Mode and the physical address assigned during Discovery Mode.

814 Discovery Mode follows the sequence listed below. Figure 6-1 shows a timing diagram of the Discover Mode for a 4
815 device segment.

- 816 1. The master powers up the bus segment to a known state.
- 817 2. The Master transmits the Discovery Command as described in Table 6-2 and shown in Figure 6-1.
- 818 3. After a predetermined delay ($t_{\text{Disc_dly}}$), all devices without a physical address activate a current ramp to the 2x
819 response current.
- 820 4. Each device monitors the current through its sense resistor (ΔI_{SENSE}).
 - 821 a. If the current is above I_{RESP} , the device disables its response current, increments its physical address
822 counter and waits for the next Discovery Command.
 - 823 b. If the current is less than I_{RESP} , the device continues to ramp its response current to $2 * I_{\text{RESP}}$ in time
824 $t_{\text{DISC_Act}}$ and maintains the current at $2 * I_{\text{RESP}}$ for time $t_{\text{DISC_Accept}}$.
 - 825 c. After time $t_{\text{DISC_Accept}}$, if a device has not detected a current through its current sense resistor of I_{RESP} or
826 greater, the device accepts physical address '1' and disables its response current.
- 827 5. After a pre-defined period ($t_{\text{Disc_Per}}$), the master transmits another "Discovery Command".
- 828 6. The devices repeat steps 3 and 4 with the device accepting the address in its address assignment counter if the
829 sense current is low.
- 830 7. The Master repeats step 5 until it has transmitted discovery commands for all the devices it expects on the bus.
- 831 8. Device initialization can now begin.



832

833

834

Figure 6-1: Discovery Mode Example for a 4 Device Bus Segment

| Item | Characteristic / Symbol | Condition / Notes | Min | Typ | Max | Unit |
|------|---|---|-----|-----|-------------------|----------|
| 51. | Time from Power Applied to First Discovery Command (t_{Disc_Start}) | Determined by the Master Clock Tolerance | 5 | | | ms |
| 52. | Slave Discovery Window (Time from Power Applied until Discovery is Ignored) (t_{Disc_End}) | Measured at the Slave | | | 12 | ms |
| 53. | Discovery Command Pulse Width (t_{Disc_Pulse}) | Determined by the Master Clock Tolerance | | 16 | | μ s |
| 54. | Slave Discovery Response Current Delay Time (t_{Disc_dly}) | Measured at the Slave | | 64 | | μ s |
| 55. | Slave Discovery Response Current Ramp Time (t_{Disc_Act}) | Measured at the Slave | 16 | | | μ s |
| 56. | Slave Discovery Response Current Activation Time (t_{Disc_Accept}) | Measured at the Slave | | | 32 | μ s |
| 57. | Discovery Period (t_{Disc_per}) | Determined by the Master Clock Tolerance | | 125 | | μ s |
| 58. | R_{S_Total} | Total Slave Current Sense Resistance on One Bus | | | \uparrow 1 (15) | Ω |

835

Table 6-2: Discovery Mode Parameter Table

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836

7 Slave Memory Map

837 The DSI3 Slave Memory Map is divided into 16 byte pages. The data types for each page are defined in Table 7-1
838 below.

| Page Address | Description |
|--------------|---|
| \$0x | Device Traceability Information |
| \$1x | Protocol Information and Settings |
| \$2x | Device Specific (Example: Device Settings and Status) |
| \$3x | Device Specific (Example: Data Source 1 Specific Information) |
| \$4x | Device Specific (Example: Data Source 1 Specific Information) |
| \$5x | Device Specific (Example: Data Source 2 Specific Information) |
| \$6x | Device Specific (Example: Data Source 2 Specific Information) |
| \$7x | Device Specific (Example: Test Mode Information) |
| \$80 - \$FF | Device Specific |

839

Table 7-1: DSI3 Required Registers - Slave

7.1 Required Slave Registers

841 Table 7-2 includes the registers and addresses which all DSI3 slaves must support.

| Register Address (Hex) | Register Name | Description | Register Size (Bits) | Register Type |
|------------------------|---------------|---------------------------------|----------------------|-----------------------------|
| \$00 | ICTYPEID | IC Type Identifier | 8 | Read Only |
| \$01 | ICMFGID | IC Manufacturer ID | 8 | Read Only |
| \$02 | ICREV | IC Silicon Revision ID | 8 | Read Only |
| \$03 | MODTYPE | Module Type Identifier Low Byte | 8 | One Time Programmable (OTP) |
| \$04 | MODMFGID | Module Manufacturer ID | 8 | One Time Programmable (OTP) |
| \$05 | MODREV | Module Revision ID | 8 | One Time Programmable (OTP) |
| \$10 | DSIREV | DSI Protocol Revision Supported | 8 | Read Only |
| \$11 | PHYSADDR | Physical Address | 8 | Read/Write or OTP |

842

Table 7-2: DSI3 Required Registers - Slave

843

844 **7.1.1 ICTYPEID Register**

845 The ICTYPEID Register defines the type of IC implemented in the slave as shown in Table 7-3.

| IC Type | Register Value (HEX) |
|-----------------|----------------------|
| Not Applicable | \$00 |
| Inertial Sensor | \$01 |
| Pressure Sensor | \$02 |
| TBD | \$03 - \$FE |
| Not Applicable | \$FF |

846 **Table 7-3: ICTYPE Register Defined Values**847 **7.1.2 ICMFGID Register**

848 The ICMFGID Register defines the type of IC manufacturer as shown in Table 7-4.

| IC Manufacturer | Register Value (HEX) |
|-----------------|----------------------|
| Not Applicable | \$00 |
| DENSO | \$01 |
| Freescale | \$02 |
| TRW | \$03 |
| TBD | \$04 - \$FE |
| Not Applicable | \$FF |

849 **Table 7-4: ICMFGID Register Defined Values**850 **7.1.3 ICREV Register**851 The ICREV Register defines the IC silicon revision. The upper byte indicates the full silicon revision and the lower
852 byte indicates the partial silicon revision.

853

854 **7.1.4 MODTYPE Registers**

855 The MODTYPE Register defines the type of slave module as shown in Table 7-5.

| Module Type | Register Value (HEX) |
|----------------------------|----------------------|
| Not Applicable | \$00 |
| Inertial Sensor | \$01 |
| Dual Axis Inertial Sensor | \$02 |
| Three Axis Inertial Sensor | \$03 |
| TBD | \$04 - \$10 |
| Pressure Sensor | \$11 |
| TBD | \$12 - \$FE |
| Not Applicable | \$FF |

856 **Table 7-5: MODTYPE Register Defined Values**857 **7.1.5 MODMFGID Register**

858 The MODMFGID Register defines the slave module Manufacturer ID as shown in Table 7-6.

| Module Manufacturer | Register Value (HEX) |
|---------------------|----------------------|
| Not Applicable | \$00 |
| DENSO | \$01 |
| Freescale | \$02 |
| TRW | \$03 |
| TBD | \$04 - \$FE |
| Not Applicable | \$FF |

859 **Table 7-6: MODMFGID Register Defined Values**860 **7.1.6 MODREV Register**

861 The MODREV Register defines the module revision level.

862 **7.1.7 DSIREV Register**

863 The DSIREV Register defines the DSI protocol revision supported as shown in Table 7-7.

| DSI Protocol Revision | Register Value (HEX) |
|-----------------------|----------------------|
| Not Applicable | \$00 |
| DSI3 | \$01 |
| TBD | \$02 - \$FE |
| Not Applicable | \$FF |

864 **Table 7-7: DSIREV Register Defined Values**

865 **7.1.8 PHYSADDR Register**

866 The PHYSADDR Register contains the Physical Address of the slave. This register can be either a one-time
 867 programmable register for slaves with pre-programmed addresses, or a Read/Write register for daisy chain connected
 868 slaves. Physical Addresses are described in Section 6.2.

869 **7.2 Required Slave Data**

870 Table 7-8 includes the data which all DSI3 slaves must support. The location and size of this data can be determined
 871 by the ICTYPE and MODTYPE registers values and thus, is not specified by this standard.

| Device Type | Page Location | Description | Minimum Data Size (Bits) | Data Type |
|-------------|---------------|--|--------------------------|--------------|
| All | Page 0 | IC Serial Number | 32 | Read Only |
| All | Page 2 | Error Detection Details | N/A | Read Only |
| Data Source | Page 1 | Periodic Data Collection Mode: Enable | N/A | Read / Write |
| | Page 1 | Periodic Data Collection Mode: Response Start Time | N/A | Read / Write |
| | Page 1 | Periodic Data Collection Mode: Response Configuration | N/A | Read / Write |
| | Page 1 | Background Diagnostic Mode: Enable | N/A | Read / Write |

872

Table 7-8: DSI3 Required Registers - Slave